

REMARKS

Applicants respectfully request reconsideration of this application as amended. Claims 1 through 7 and claims 15 through 23 are presented for examination. Claims 8 through 14 were previously withdrawn without prejudice to future prosecution. New claims 20 through 23 have been added. Examination of new claims 20 through 23 is requested.

SECTION 112 ISSUES

In the Final Office Action, claims 2 through 4 and claims 16 through 19 stand rejected under 35 U.S.C. § 112, second paragraph. Applicants respectfully traverse.

In the Final Office Action, under paragraph (a) of the rejections under 35 USC § 112, it is stated that "it is not clear whether applicants mean the gate electrode or the region surrounding the gate." In an effort to more particularly and distinctly claim the present invention, applicants have amended claims 2 through 4 to now recite in pertinent part "diffused gate region material". Claim 16 has been amended to now recite in pertinent part "diffused gate region". Additionally claims 1 and 15 have been amended to now recite in pertinent part "a metallic gate electrode". Applicants believe that this terminology is now in agreement with the exemplary "gate region" disclosed in reference to Figure 1 (gate region 110) and in reference to Figure 5 (gate region 510), both of which show a diffused gate region above a gate insulator area. At the same time the use of "metallic gate electrode" now more clearly is directed to the exemplary gate electrode 112 of Figure 1 and gate electrode 522 of Figure 5. Applicants submit that the recitations of "diffused gate region material" and "diffused gate region" in claims 2, 3, 4, and 16 are not now indefinite when read in light of the specification and drawings. Furthermore the distinction

between the metalization contact "metallic gate electrode" and the semi-conductor deposited or diffused "diffused gate region" is now more clearly made. Therefore applicants respectfully request that the rejection under 35 USC 112, second paragraph, be withdrawn.

In the Final Office Action, under paragraph (b) of the rejections under 35 USC § 112, it is stated that "should claims 1 – 7 be found to be allowable, claims 15 – 19 will be objected to under 37 CFR § 1.75 as being a substantial duplicate thereof." In an effort to more particularly and distinctly claim the present invention, applicants have amended claim 1 to now recite in pertinent part "with a shifted *during manufacture* flat band magnitude." (Applicants' emphasis added.) Applicants have not amended claim 15 to contain the recitation "during manufacture". Applicants believe that the additional limitation "during manufacture" in claim 1 and thereby in the claims depending from claim 1, claims 2 through 7, make claims 1 through 7 patentably distinct from claims 15 through 19. Therefore applicants respectfully request that the rejection under 35 USC § 112, second paragraph, be withdrawn.

SECTION 103 ISSUES

In the Office Action, claims 1 through 7 and claims 15 through 19 stand rejected under 35 U.S.C. § 103(a) as being anticipated by, among other references, *Stein, et al.*, U.S. patent number 4,055,837 (Hereinafter *Stein*). Applicants respectfully traverse.

"To establish a *prima facie* case of obviousness, three basic criterion must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.” (MPEP section 2142 August 2001, citing decisions including *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991).)

Applicants respectfully submit that a *prima facie* case of obviousness has not been made in the Office Actions of 11/05/01 and 06/11/02. Applicants first consider the third requirement that the prior art reference (or references when combined) must teach or suggest *all* the claim limitations.

Amended independent claim 1 now recites in pertinent part “a *metal-oxide-semiconductor transistor* with a shifted during manufacture flat band magnitude.” (Applicants emphasis added.)

The 11/05/01 Office Action stated that “*Stein* describes an apparatus (device) including a MOS transistor (fig. 1 31, col. 2 lines 7-8) with a shifted band flat band magnitude (col. 7 lines 32-35)”. Applicants respectfully submit that *Stein* at Figure 1 actually discloses *two distinct structures*, a metal-oxide-semiconductor (MOS) transistor, item reference 1, and a stand-alone metal-nitride-oxide-semiconductor (MNOS) capacitor, item reference 2. Specifically, *Stein* recites at column 2, lines 6 through 11:

A single-transistor memory element, as best seen in FIG. 1, comprises a transistor 1 and a capacitor means 2 connected in series. The transistor 1 is a MOS field-effect transistor.

The capacitor means 2 comprises a capacitor whose dielectric comprises rechargeable states, being a MNOS capacitor.

Any reference to a shifted flat band magnitude within *Stein* is in connection to *MNOS capacitor* 2, and never in connection with *MOS transistor* 1.

The Office Action reference to *Stein* column 7, lines 32 through 35, is clearly in regards to a capacitor, not a MOS transistor. Claim 20 of *Stein* recites in pertinent parts "for the operation of a single-transistor memory element ... comprising a write line, a transistor, and a capacitor ... such that where of an information '0' is stored in said capacitor a shifting of a flat-band voltage occurs" This recitation indicates that it is *within the capacitor*, and not *within the transistor*, that any shifting of a flat-band voltage occurs.

Similarly claim 19 of *Stein* recites "such that flat-band voltage of said capacitor is shifted" (column 7, lines 8 and 9), and claim 22 of *Stein* recites "and in a case of the shifted flat-band voltage of the capacitor" (column 8, lines 23 and 24). Within the specification of *Stein*, applicants point out at column 2, line 68, through column 3, line 2, the following recitation: "[t]his means that the states ('traps') of the MNOS capacitor are recharged and that the flat-band voltage of the capacitor is shifted." Similarly *Stein* recites at column 3, lines 34 through 37, "a reloading of the states in the dielectric of the memory capacitor will be effected causing a prospective shift in the flat-band voltage." Thus *Stein* only discloses a "shift of a flat-band voltage" in relation to a *capacitor*, and never in relation to a *transistor*. However, claim 1 of the present application recites in pertinent part "a metal-oxide-semiconductor *transistor with a shifted during manufacture flat band magnitude*." (Applicants emphasis added.) Applicants submit that *Stein* neither teaches nor suggests such a metal-oxide-semiconductor transistor with a shifted at manufacture *flat band magnitude*.

Furthermore, the *Stein* reference only discloses a "shift of a flat-band voltage" in relation to a capacitor *during operation*. (See *Stein* col. 2 lines 53 – 59; col. 3 lines 1 – 2; col. 3 lines 34 – 41; and col. 3 lines 54 – 58.) However claim 1 of the present application recites in pertinent part

“a metal-oxide-semiconductor transistor with a *shifted during manufacture flat band magnitude*.” (Applicants emphasis added.). Applicants submit that *Stein* neither teaches nor suggests such a metal-oxide-semiconductor transistor *with a shifted at manufacture flat band magnitude*.

Therefore, applicants submit that the first element of claim 1 is not taught or suggested by *Stein*.

Amended independent claim 1 now recites in pertinent part “a metallic source electrode, a metallic drain electrode, and a substrate electrode *of said metal-oxide-semiconductor transistor* coupled to each other and to a negative voltage source.” (Applicants emphasis added.)

The 11/05/01 Office Action stated that these three elements were comparable to items 31, 13, and 5 of Figure 2 of *Stein*. Applicants respectfully submit that item 5 is not a *substrate electrode* but rather the *substrate* itself. In fact *item 4* of Figure 2 is the substrate electrode, and it is coupled to a negative voltage source. However, item 4 is not coupled to items 31 and 13. If the argument of the 11/05/01 Office Action is that MOS transistor (item 1 of *Stein*) is the metal-oxide-semiconductor transistor as recited in claim 1, then applicants submit that the source electrode, drain electrode, and substrate electrode of said metal-oxide-semiconductor transistor are *not* coupled to each other as recited in claim 1. If on the other hand the argument of the 11/05/01 Office Action is that NMOS capacitor (item 2 of *Stein*) is the metal-oxide-semiconductor transistor as recited in claim 1, then clearly the drain electrode 31 is not “of” NMOS capacitor. In neither argument made in the 11/05/01 Office Action do the source electrode, drain electrode, and substrate electrode of *Stein* teach or suggest the recited claim elements of claim 1.

Therefore, applicants submit that the third, fourth, and fifth elements of claim 1 are not taught or suggested by *Stein*.

For the above reasons, applicants submit that the recited claim elements of claim 1 are neither taught nor suggested by *Stein*. Therefore applicants submit that the Office Actions of 11/05/01 and 06/11/02 have not presented a proper *prima facie* case of obviousness for claim 1. Applicants submit that the invention of claim 1 is not rendered obvious by *Stein*, and should be allowed as non-obvious in light of the cited art of record.

Claims 2 through 7 depend from independent claim 1. Since independent claim 1 is believed allowable as non-obvious in light of the prior art of record, applicants submit that claims 2 through 7 are also allowable.

Once amended independent claim 15 now recites in pertinent part "means for shifting a flat band magnitude in a metal-oxide-semiconductor transistor." The Office Action of 11/05/01 states that "claim 15 repeats the elements of claim 1 ... and claims 15 – 19 are rejected for reasons stated under claims 1 – 5 above." The Office Action of 11/05/01 apparently argues that the MNOS capacitor (*Stein* item 2), either by itself or on conjunction with MOS transistor (*Stein* item 1,) would supply the means for shifting a flat band magnitude.

However, the recited element of claim 15 is presented in means-for language. Under 35 USC § 112, sixth paragraph, such a claim element "shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." The Court of Appeals for the Federal Circuit has stated that "the 'broadest reasonable interpretation' that an examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification

corresponding to such language when rendering a patentability determination.” *In re Donaldson Co.*, 16 F.3d 1189 (Fed. Cir. 1994).

Applicants freely submit that no NMOS capacitor, such as that disclosed in item 2 of *Stein*, is disclosed in the present application. Neither has the Office Action presented a rationale for why an NMOS capacitor is equivalent to the structure that is disclosed in the present application for the means for shifting a flat band magnitude. For this reason, the NMOS capacitor of *Stein* does not teach or suggest the recited claim elements of claim 15.

Therefore applicants submit that the Office Actions of 11/05/01 and 06/11/02 have not presented a proper *prima facie* case of obviousness for claim 15. Applicants submit that the invention of claim 15 is not rendered obvious by *Stein*, and should be allowed as non-obvious in light of the cited art of record.

Claims 16 through 19 depend from independent claim 1. Since independent claim 1 is believed allowable as non-obvious in light of the prior art of record, applicants submit that claims 16 through 19 are also allowable.

SUMMARY

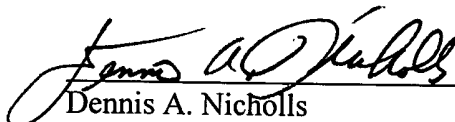
Applicants believe that all pending claims are allowable over the cited art of record. Applicants therefore respectfully request that all pending claims 1 through 7 and 15 through 23 be allowed.

If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to contact applicant's representative, Dennis A. Nicholls, at (408) 765-5789.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

Date: 11 September 2002

A handwritten signature in dark ink, appearing to read "Dennis A. Nicholls", written over a horizontal line.

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VERSION WITH MARKINGS TO SHOW CHANGES

112C(1) - no support
- 112C(2)?
indep in 6

1. (Once amended) An apparatus, comprising:

a metal-oxide-semiconductor transistor with a shifted during manufacture flat band magnitude;

a metallic gate electrode coupled to said metal-oxide-semiconductor transistor and to a positive voltage source; and

a metallic source electrode, a metallic drain electrode, and a substrate electrode of said metal-oxide-semiconductor transistor coupled to each other and to a negative voltage source.

not
given
particular
weight

2. (Twice amended) The apparatus of claim 1, wherein said metal-oxide-semiconductor includes a diffused gate region material with a work function less than - 0.56 volts.

3. (Twice amended) The apparatus of claim 2, wherein said diffused gate region material is platinum silicate.

4. (Twice amended) The apparatus of claim 2, wherein said diffused gate region material is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

15. (Once amended) An apparatus, comprising:

means for shifting a flat band magnitude in a metal-oxide-semiconductor transistor;

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means for coupling a metallic gate electrode of said metal-oxide-semiconductor transistor to a positive voltage source; and

means for coupling a metallic source electrode, a metallic drain electrode, and a substrate electrode of said metal-oxide-semiconductor transistor to a negative voltage source.

16. (Twice amended) The apparatus of claim 15, wherein said means for shifting includes a diffused gate region with a material whose work function is less than -0.56 volts.